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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/507,117 | 09/10/2004 | Hiroyuki Takahashi | 029471-0168 | 4725 |

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| EXAMINER | |
|---|---|
| HUR, JUNG H | |
| ART UNIT | PAPER NUMBER |
| 2824 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/507,117 | TAKAHASHI ET AL. | |
| | Examiner | Art Unit | |
| | Jung (John) H. Hur | 2824 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-37,40,42-48 and 52-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-37,40 and 42-48* is/are allowed.

6)☒ Claim(s) *52-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Amendment***

1. Acknowledgment is made of applicant's Amendment, filed 20 November 2006. The changes and remarks disclosed therein have been considered.

Claims 1, 38, 39, 41, 49-51 have been cancelled and claims 52-55 have been added by Amendment. Therefore, claims 2-37, 40, 42-48 and 52-55 are pending in the application.

***Specification***

2. Claims 3, 10, 45, 46, 52, 53 and 55 are objected to because of the following informalities:

In claim 3, line 3 and claim 10, line 4, "an array from" should be --an array form--.

In claim 10, lines 10-11, "for supplying a relatively high power supply voltage" is understood as --including a relatively high voltage power supply-- (to be consistent with "a relatively low voltage power supply" in line 11).

In claim 10, lines 17-18, "the supplied power supply voltage" and "the power supply voltage" are understood as --the provided power supply voltage-- (see also, as a reference, claims 3, 6 and 7).

In claim 45, line 14, "a constant voltage" should be --the constant voltage-- (see also claim 46).

In claim 45, line 17, "the power supply voltage" is understood as --the provided power supply voltage-- (see also, as a reference, claims 42-44).

In claim 46, line 13, "the power supply voltage" is understood as --the provided power supply voltage-- (see also, as a reference, claims 42-44).

In claim 52, line 10, claim 53, line 7, and claim 55, line 8, "an output voltage" should be --the output voltage--.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 52-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,222,044 (Tsujimoto) in view of U.S. Pat. No. 5,307,315 (Oowaki et al.).

Regarding claim 52, Tsujimoto, for example in Figs. 5-8, discloses a semiconductor memory device comprising: a memory cell array having a plurality of memory cells arranged in an array form (M11-Mmn in Fig. 5); a word line driving circuit (within 53 in Figs. 5 and 7) receiving a constant voltage (Vh in Fig. 8, from 53a in Fig. 5) as a driving voltage and driving a selected word line (among WL1-WLm) by the constant voltage (see WORD LINE in Fig. 8); a sense amplifier (among SA1-SAn in Figs. 5 and 6) amplifying a high level voltage of a selected bit line to a provided power supply voltage (Vext; see SENSE AMPLIFIER CIRCUIT in Fig. 8), and voltage step down circuit (63) outputting a voltage (Vint in Fig. 8) that is lower than said power supply voltage (Vext), wherein said memory cell array is driven by the output voltage from said voltage step-down circuit (via 54 in Figs. 5 and 7; see also, as a reference, Figs. 6 and 14 of the instant application).

Tsujimoto does not expressly disclose that said constant voltage does not depend on said provided power supply voltage.

Oowaki discloses, for a word line driving circuit (within 14 in Fig. 1), a constant voltage (Vbw in Fig. 1, or Vwd in Figs. 2, 5 and 6) that does not depend on a provided power supply voltage (VCC in Figs. 2 and 6; Fig. 6 shows a constant Vwd for a range of VCC).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the Oowaki's means for generating a word line driving voltage for the Tsujimoto's word line driving circuit (for example, within 53a in Figs 5 of Tsujimoto), such that the constant voltage of Tsujimoto would not depend on the provided power supply voltage (as in Oowaki), for the purpose of consistently providing high-performance, reliable memory operations, including word line driving operations, that are insensitive to variation in the external power supply voltage (see for example Oowaki, Abstract, lines 9-19 and column 2, line 55 through column 3, line 9).

Regarding claim 53, the above combination discloses the semiconductor memory device according to claim 52, further comprising: a peripheral circuit (56 in Fig. 5 of Tsujimoto) which comprises a circuit (for example, 56b) that generates a signal for determining the transition timing of a control signal for said memory cell array and/or the pulse width of the control signal (see, for example, TRANSFER GATE CONTROLLING SIGNAL in Fig. 8 of Tsujimoto); said circuit being driven by the output voltage from said step down circuit (for example, 56b driven by the output of 63 in Figs. 5 and 7 of Tsujimoto).

The above combination does not expressly disclose that said peripheral circuit comprises a delay circuit that delays a received signal; said delay circuit being driven by the output voltage from said step down circuit.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include a delay circuit in the peripheral circuit of Tsujimoto (for example, for the pulse width and/or the transition timing of the output of 56b in Fig. 8 of Tsujimoto), such that said delay circuit would be driven by the output voltage from said step down circuit (since 56b is driven by the step down voltage in Figs. 5 and 7 of Tsujimoto), since use of a delay circuit for a pulse width or a transition timing was common and well known in the art.

Regarding claims 54 and 55, the above combination discloses the semiconductor memory device according claim 53:

wherein said peripheral circuit is driven by said power supply voltage (see, for example, 56a and 56c in Figs. 5 and 7 of Tsujimoto);

further comprising: a reference voltage circuit (44 or 46 in Figs. 2 and 3 of Oowaki, as applied to the above combination) that generates a reference voltage (Vr1 or Vr2); and a voltage step up circuit (including 26 in Figs. 1 and 2 of Oowaki) that receives said reference voltage and outputs a step up voltage (Vwd in Fig. 6 of Oowaki, corresponding to Vh in Fig. 8 of Tsujimoto) wherein said step up voltage is supplied to said word line driving circuit; said step up voltage is supplied to a selected word line of said memory cell array (see for example Fig. 8 of Tsujimoto); and said reference voltage circuit and said step up circuit are driven by the output voltage from

said step down circuit (see Fig. 5 of Tsujimoto, showing 53a driven by the step down voltage from 63, as applied to the above combination).

### *Allowable Subject Matter*

5. Claims 2-37, 40 and 42-48 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 3, 42, 45 and 46 (and the corresponding dependent claims), the record of the prosecution as a whole makes clear the reasons for the indication of allowable subject matter. See the previous Office Action, mailed 22 August 2006.

Regarding claim 10, the prior arts of record do not disclose or suggest a semiconductor memory device as recited in claim 10, *in toto*, and particularly, in conjunction with other limitations, a delay circuit having a characteristic in which a delay time thereof becomes shorter when the provide power supply voltage is low than when the provided power supply voltage is high.

### *Conclusion*

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) H. Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jhh

1/30/07

JUNG (JOHN) H. HUR
PRIMARY PATENT EXAMINER